Design for Test (DFT) Guidelines

Contents

Scope

This document has been produced as a reference for circuit board designers who wish to enhance in-circuit test (ICT) coverage of a given design before boards go into volume production.

Specific tester related topics refer to the Teradyne 18xx series, although the general rules and guidelines will be true of any test system.

Introduction

An In-Circuit test system has three basic elements: the tester itself; a vacuum test fixture for each board type; and a test program for each board type.

The tester can be regarded as a computer block which allows the other two elements to be integrated with it. It has an operator interface which allows the test to be started and a display and printer to display the test results. The operator is normally an unskilled person, required only to load PCB assemblies onto the test fixture and initialize the test itself.

The vacuum test fixture consists of a number of spring-loaded probes housed in a construction of metal and fibre glass which make contact with one point on each circuit node (electrical network) when the board is sucked down onto them. A node is defined as a set of one or more component leads that are electrically connected together. Only one point on each node will be probed, unless specific pieces of PCB track are required to be tested. It is important that a good vacuum seal is achieved (if vacuum is applied directly to the PCB) and that the probes find their targets accurately.

The test program is designed to isolate each component, in turn, from the surrounding circuit and to test it as if it were a single component. Where this is not possible (e.g. capacitors in parallel), a group of components is tested or allowances made for interfering components that cannot be isolated. Generally a test program will first check probe contact, check for known continuities and for shorts (between all other nodes), test each discrete component, apply power to the board and then test ICs. If a failure is detected in one of these sections, the succeeding sections will not be executed and a failure message will be displayed to the operator and a ticket printed showing the failing component(s). This is so that false failures and possible board/component damage is kept to a minimum.

Fortunately, with modern In-Circuit ATE systems there are relatively few design constraints when they are compared with older, functional test systems. The constraints that do exist, however, can render a board untestable if they are not followed, or at best very difficult (and expensive) to test.

Board Layout Constraints

1. Always provide two tooling holes on the board, preferably in diagonally opposite corners. These holes should be 3-4mm. in diameter and ideally have a tolerance of +0.05mm/-0.00mm. They may be plated through, but the tolerance must be maintained. The tolerance of the pitch between the tooling holes is important (to achieve the accurate targeting required) and should be maintained at +/-0.125mm. It is vital to ensure perfect tooling hole registration with the tracking so that all test probes can find their target repeatedly.

2. It is not generally advisable to have probes placed at less than 0.1 in. from each other or from a component lead. When using components with a lead pitch less than this and where there are no other places to probe on the same node, provide dummy plated through holes or test lands connected to, but away from each lead, staggering them if necessary, such that this design rule is not contravened.

3. Except for SMDs, avoid fitting components deeper than 2MM to the underside of the board. This helps the fixture manufacturer and avoids possible component damage on mis-loaded boards.

4. All nodes should be accessible from the non-component side of the board, where probing occurs. It is possible to probe on both sides of the board, but it is more expensive. Top probing has to be employed when full underside probing cannot be provided. When using SMDs, ensure that sufficient dummy plated through holes or test lands are provided to ensure that this may be achieved. A test land of at least 0.04" diameter is the preferred method of probe to PCB connection.

5. A standard test fixture uses a grid of pushers mounted above the PCB assembly to push the board onto the test probes. This method has many advantages over applying vacuum to the underside of the PCBA, including:-

   - Open via holes and other gaps do not compromise vacuum seal
   - The board is uniformly pressed down, keeping level at all times during the cycle, even if large clusters of test probes are present.
   - There is no edge seal to wear out

   The only constraint associated with this method is that sufficient room is made available on the top side of the PCB between components for the pushers. A typical pusher is 6MM diameter, but they can be made tapered to fit any available space, down to 2MM. Pushers are not applied to component surfaces to avoid component damage and possible false passes (pressure applied to an IC with an open/bent lead may cause a false pass).

Circuit Design Constraints

1. Ensure that all electrical nets (whether actively used or not) are made available for probing so that full shorts coverage can be achieved. This would include nets on things such as unused pins on connectors, elements of R-Packs or Logic gates. Genuinely not connected (i.e. no internal connection) pins of ICs could be omitted.

2. To prevent device damage during the isolation process, digital devices must operate at the standard TTL voltage levels (+5v and 0v). This does not preclude the use of CMOS devices, just run them from a +5v supply. 3V logic systems are supported if the target tester has the 3V PSU option fitted.

3. Never tie the output enable pins of tri-state devices directly to a supply rail, connect them instead via individual resistors. The ATE system must be able to disable these devices when it needs to so that other devices connected to the same nets do not interfere with either the stimulus or the measurement of a given device.

4. In designs incorporating microprocessors, if the support chips are enabled directly from non-exclusively decoded address lines or directly from control signals, always include a buffering stage on these signals that can be disabled. You could use a tri-state buffer, for example, with the output enable pin tied via a resistor to the appropriate supply rail. Alternatively, a dual input AND gate could be used, with the spare input connected via a resistor to the +5v rail. In both examples the ATE system can isolate the processor from the surrounding circuit by holding the tied pin. This is most important if the processor itself is to be tested as the system supplies instructions to the processor on its data bus because if the surrounding circuit responds to the processor signals, bus contentions may occur.

5. Where the design incorporates a free running clock, incorporate a buffer stage that may be disabled at the source of the clock (refer to rule 3 for possible methods). This also applies to clock signals from processors (e.g. CLKOUT from 80186).

6. If a device is fed from a TTL clock instead of a crystal, include extra stages in the clock circuit that allow the original clock to be disabled and an ATE system clock source to be inserted.. TTL oscillators with built in output enable are also an option. Refer to appendix 1.1 for an example.

7. Always show spare / not connected pins of ICs, etc, on the circuit diagram and in the netlist. These pins can then have nodes assigned to them and be included in the tests. Always tie the inputs to a supply via a resistor - especially important for CMOS type devices which may oscillate if inputs are left floating.

8. Avoid using large value capacitors (greater than 1uF say) on signal lines. Generate a power on reset signal with a smaller cap and a suitable resistor to achieve the required time constant. This is because when the tester stimulates these lines the capacitance may adversely affect its signals.

9. Zener diodes are tested in the unpowered cycle of the test. Therefore any large value Zener attached directly to an unpowered IC might cause damage to that IC. A series resistor between IC and Zener would allow 'guarding' of the IC pin and hence avoid possible damage.

10. If 'Capscan', 'Wavescan', 'Framescan' or 'Framescan' Plus test techniques are to be used, space for the sensor should be available above that device. Capscan tested capacitors should be in a repeatable position so that the sensor can always touch the component.

ICT Generation Requirements

Before work can commence on the design of a fixture and test program for a new product, several items must be supplied and they MUST be of the correct production issue.

1. Circuit diagram.
2. Parts list (BOM). This must include details of component value and tolerance.
3. Bare board manufactured to the correct level.
4. Loaded board constructed to the level at which it is to be tested, including build variants. Towards the end of program development, more samples will be required to verify test repeatability.
5. Board outline drawing, showing dimensions and tolerances of the board and tooling holes.
6. CAD netlist and drilling file (Ascii format file showing tooling hole positions and test point / component lead positions).
7. Any specific component testing requirements.
8. Details of target tester.

In order to generate a quotation for a given job, all items apart from items 3 and 4 are required.